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**Areas of interest** are Nanoelectronics, Nanoscale MOSFET modeling and simulation, Design and Development of low power novel devices, FinFET based Memory Design, Emerging Devices in Analog Design, and Design and development of reconfigurable logic. He has guided 14 Ph.D. scholars. Currently, he is supervising around six candidates leading to their Ph.D. degrees. He has been nominated for INAE Young Engineer Award and acted as a reviewer for IEEE Transactions on Electron Devices, IEEE Electron Device Letters, IEEE Transactions on Nanotechnology, Superlattice and Microstructures, International Journal of Electronics, Semiconductor Science and Technology, Nanotechnology, IEEE Transactions on VLSI Systems, Microelectronic Engineering, Microelectronic Reliability amongst other. He is a part of TPC as a Track Chair for VLSI-D 2017, 2018, and 2019.

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