Curriculum Vitæ

Jawar Singh

Professor

Birth	August 15, 1977
Nationality	INDIAN
Address	Department of Electrical Engineering Indian Institute Technology Patna Patna, Bihar, INDIA, 801106
Mobile	+91-9425802562
E-Mail	dr.jawar@gmail.com jawar@iitp.ac.in

APPOINTMENTS

Project Director, Technology Innovation Hub 2022–
Indian Institute of Technology Patna, INDIA

Professor, Department of EE 2022–
Indian Institute of Technology Patna, INDIA

Associate Dean, Research & Development 2021–2022
Indian Institute of Technology Patna, INDIA

Associate Professor, Department of EE 2017–2022
Indian Institute of Technology Patna, INDIA

Associate Professor, Department of ECE 2013–2017
Indian Institute of Information Technology, D & M Jabalpur, MP, INDIA

Assistant Professor, Department of ECE 2011–2013
Indian Institute of Information Technology, D & M Jabalpur, MP, INDIA

Assistant Professor, Department of ECE 2010–2011
Jaypee University of Engineering and Technology, Guna, MP, INDIA

Lecturer, Department of EE 2002–2006
Madhav Institute of Technology and Science (MITS), Gwalior, MP, INDIA

VISITING RESEARCHER/POST-DOCTORAL FELLOW

Visiting Researcher, Department of CSE, (six months) 2016
University of North Texas, Discovery Park, Danton, TX 76207 USA
Host Mentor: Professor Saraju Mohanty

Visiting Researcher, Department of CSE, (six months) 2009/10
Pennsylvania State University, University Park, PA 16802 USA
Host Mentor: Professor Vijaykrishnan Narayanan

EDUCATION

PhD Computer Science and Engineering 2006-2010
University of Bristol, Bristol, United Kingdom (UK)
Thesis advisor: Professor Dhiraj K Pradhan
Thesis Title: Low Power SRAM Design and Analysis

M.Tech. Measurement and Instrumentation 1999-2001
Indian Institute of Technology (IIT), Roorkee, INDIA
Thesis advisor: Professor R S Anand
Thesis Title: Computer Aided Analysis of Phonocardiogram

B. Engg. Electrical Engineering 1995-1999
Madhav Institute of Technology and Science (MITS), Gwalior, MP, INDIA
(an autonomous MP State Government Institute)

RESEARCH INTEREST

- Neuromorphic and In-memory Computing Device & Circuits
- Exploration and investigation of emerging devices for analog and digital domain
- Design and development of RF energy harvester for IoT applications
- Integrated Circuits security and PUF design
- Modeling, simulation and characterization of emerging devices
- Low power high speed volatile and non-volatile memory design
- Process variation and fault tolerant VLSI system design
- Aging and radiation hardened system design

AWARDS AND FELLOWSHIP

- 2020 Elevated as Fellow IE (India)
- 2020 Elevated as Fellow IETE
- 2016 BHAVAN (Indo-US) Fellowship for six months at the University of North Texas, Denton, USA

- 2015 Best Paper Award, IEEE International Symposium on Nanoelectronic and Information Systems, INDIA
- 2014 Travel grant from SERB (Department of Science and Technology, Govt. of INDIA) for attending an International conference in Santa Clara, CA, USA
- 2014 Elevated to Senior Member IEEE (92189326), IEEE USA
- 2012 Inventor Incentive Award, the Pennsylvania State University, USA
- 2009 Worldwide University Network Fellowship, Government of UK
- 2005 National Overseas Fellowship, Government of INDIA
- 1999 GATE Scholarship

FUNDING AND RESEARCH PROJECTS

- Indian Institute of Remote Sensing, Govt. of INDIA, "Artificial Intelligence Powered Remote Sensing Based Lightning and Hailstorm Alert System", 37, 60, 000 (Co-PI, 2022 – 2025).
- Department Science and Technology, Govt. of Bihar, "Establishing Center of Excellences in Government Polytechnic Colleges", 67 Crore (PI, 2022 – 2027).
- Science and Engineering Research Board (SERB) DST Govt. of India, "Design and Development of Silicon Artificial Neuron and Synapse for Brain Inspired Computing", 35,00,000 (PI, 2022 – 2025).
- National Mission on Interdisciplinary Cyber Physical Systems, SERB, DST Govt. of India, "Technology Innovation Hub-IIT Patna ", 110 Crore (Project Director, 2019 – 2024).
- Science and Engineering Research Board (SERB) DST Govt. of India, "Exploration of 8/9 nano-meter process variation immune doping- and junction-free devices and their circuits", 35,00,000 (PI, 2017 – 2019).
- Science and Engineering Research Board (SERB) DST Govt. of India, "Design and Development of RF Energy Harvesting Circuits for Low-power Electronic Devices ", 55,00,000 (PI, 2015 – 2018).
- Ministry Of Electronics & Information Technology (SMDP), Govt. of INDIA, "Power management module- Wireless Sensor Network node for IoT", 67,00,000 (Co-PI, 2015 – 2019).
- Ministry Of Electronics & Information Technology (SMDP), Govt. of INDIA, "Low power processor based power management unit for Internet of Things (IoT) applications", 16,95,000 (Co-PI, 2015 – 2019).
- Indian Nano-electronic User Program (INUP), IIT Bombay, "Characterization of Tunnel - FETs for low power Static RAM bitcells", 12,00,000 (PI, 2010 – 2012).
- All India Council for Technical Education, Govt. of INDIA, "Computer Aided Analysis and Diagnosis of Hansen Disease", 11,00,000 (Co-PI, 2004 – 2006).

PATENTS

4. Dhiraj K. Pradhan, Jawar Singh and Jimson Mathew, "Static Random Access Memory", *US Patent No. 7706174; issued April 27, 2010.*

3. Jawar Singh Ramakrishnan Krishnan, Saurabh Mookerjea, Suman Datta, and Vijay Krishnan Narayan, "TFET based 6T SRAM cell ", *U.S. Patent No. 8,369,134, Feb 3, 2013.*

2. Jawar Singh and Anup Shrivastav, "Resistive Switching Device: Memristor", *Indian Patent Application No. 431/MUM/2015, Feb 2015.*

1. Pandey Sandeepkumar, Zalke Jitendra and Jawar Singh, "A method and system for providing the identification, authentification and security using unique thermal profile signature map (UTPSM)", *Indian Patent Application No. 201721046615, Dec 2017.*

BOOK AND BOOK CHAPTERS

3. Jawar Singh and Chitrakant Sahu, "Nano-CMOS and Post-CMOS Electronics: Devices and Modelling, [Junction and Doping Free Transistors For Future Computing]", *IET UK, ISBN 978-1-84919-997-1, 2015.*

2. Jawar Singh and Balwinder Raj, "Embedded System / Book 1 Chapter Title [SRAM Cells for Embedded Systems]", *INTECH Open Access Publisher, ISBN 979-953-307-580-7, 2014.*

1. Jawar Singh, S. Mohanty and Dhiraj K. Pradhan, "Robust and Power-Aware SRAM Bitcell Design and Analysis", *Springer-Verlag New York Inc., Hardcover, ISBN 978-1-4614-0817-8, 2013.*

PEER-REVIEWED JOURNAL PAPERS [Google Scholar Statistics]

45. Alok Kamal, Akanksha Thakur, and Jawar Singh, "Emulating Switching from Short-Term to Long-Term Plasticity of Bio-Synapse using Split Gate MOSFET", *IEEE Transactions on Nanotechnology, August 2022.*

44. Tripty Kumari, Jawar Singh, and Pramod Kumar Tiwari, "Split-Gate Induced High-Field for Impact Ionization Triggered Bipolar Action and Sub-kT/q Switching in Junctionless FET", *IEEE Transactions on Nanotechnology, June 2022, Vol 21, pp 332 - 339.*

43. Rakesh Kumar, Meena Panchore, Lokesh Bramhane, and Jawar Singh, "Comparative Performance and Reliability Analysis of Doping and Junction Free Devices with High-k/Vacuum Gate Dielectric", *Springer Silicon, 2020.*

42. Tripty Kumari, Pramod Kumar Tiwari, Jawar Singh, Kuei-Shu Chang-Liao, "Subthreshold Modeling of GAA MOSFET Including the Effect of Process-Induced Inclined Sidewalls", *IEEE Transactions on Electron Devices, vol.68, Dec 2021 (IF 2.93).*

41. Alok Kamal and Jawar Singh, "Fully Planar Impact Ionization -RAM Cell with High-Performance and Non-Destructive Read-out", *IEEE Transactions on Electron Devices, vol.68, Sept 2021 (IF 2.93).*

40. Alok Kumar, Neha Kamal and Jawar Singh, "A low power L-shaped gate bipolar impact ionization MOSFET based capacitorless one transistor dynamic random access memory cell", *IoP Science, Japanese Journal of Applied Physics, vol.60, May 2021 (IF 1.48).*

39. Neha Kamal, Alok Kamal and Jawar Singh, "L-Shaped Tunnel Field Effect Transistor Based 1T DRAM with Improved Read Current Ratio, Retention Time and Sense Margin", *IEEE Transactions on Electron Devices, vol.68, June 2021 (IF 2.93).*

38. Kanchan Cecil, Jawar Singh, and Dip Prakash Samajdar, "Channel-hot-carrier degradation in the channel of junctionless transistors: a device- and circuit-level perspective", *Silicon (2021).*

37. Panchore Meena, Bramhane Lokesh, and Jawar Singh, "Channel-hot-carrier degradation in the channel of junctionless transistors: a device- and circuit-level perspective", *Journal of Computational Electronics, Springer Nature, 20, pp 1196–1201 (2021) (IF 1.53).*

36. Neha Kamal and Jawar Singh, "A Highly Scalable Junctionless FET Leaky Integrate-and-fire Neuron for Spiking Neural Networks", *IEEE Transactions on Electron Devices, vol.68, April 2021 (IF 2.93).*

35. Tripty Kumari, Jawar Singh, and Pramod Kumar Tiwari, "Investigation of Ring-TFET for Better Electrostatics Control and Suppressed Ambipolarity", *IEEE Transactions on Nanotechnology, vol.19, pp 829 - 836, 2020.*

34. Meena Panchore, Kanchan Cecil, and Jawar Singh, "Impact of Temporal Variability on Dopingless and Junctionless FET based SRAM Cells", *Springer Silicon, 2020.*

33. Alok Kumar Kamal, and Jawar Singh, "Simulation based Ultra-Low Energy and High Speed LIF Neuron using Silicon Bipolar Impact Ionization MOSFET for Spiking Neural Networks", *IEEE Transactions on Electron Devices, vol.67, June 2020 (IF 2.93).*

32. Md. Hasan Raza Ansari, and Jawar Singh, "Capacitorless 2T-DRAM for Higher Retention Time and Sense Margin", *IEEE Transactions on Electron Devices, vol.67, no.3, pp 6, 2020 (IF 2.93).*

31. Neha Kamal, Avinash Lahgere, and Jawar Singh, "Evaluation of Radiation Resiliency on Emerging Junctionless/Dopingless Devices and Circuits", *IEEE Transactions on Device and Materials Reliability, vol. 19, no.2, pp 728 - 732, Dec. 2019 (IF 1.58).*

30. Ankit Sirohi, Chitrakant Sahu, and Jawar Singh, "Analog/RF Performance Investigation of Dopingless FET for Ultra-Low Power Applications", *IEEE Access, vol.7, pp 141810 - 141816, August 2019 (IF 4.01).*

29. Deepti Gola, Balraj Singh, Jawar Singh and Pramod Tiwari, "Static and Quasi-Static Drain Current Modeling of Tri-Gate Junctionless Transistor with Substrate Bias Induced Effects", *IEEE Transactions on Electron Devices, vol.67, no.7, pp 2876 - 2883, May 2019 (IF 2.93).*

28. Neha Kamal, Meena Panchore, and Jawar Singh, "3-D Simulation of Junction- and Doping-free Field-effect Transistor under Heavy Ion Irradiation", *IEEE Transactions on Device and Materials Reliability, vol. 18, pp 173-179, no.2 , March 2018.*

27. Lokesh Kumar Bramhane, and Jawar Singh, "Improved performance of bipolar charge plasma transistor by reducing the horizontal electric field", *Superlattices and Microstructures (Elsevier), Vol 104, April 2017, (IF 2.13).*

26. Muhammad Khalid, Jawar Singh and Saraju P. Mohanty, "Impact of Channel Hot Carrier Effect in Junction- and Doping-Free Devices and Circuits", *Journal of Nanoelectronics and Optoelectronics, vol.12, no.1, Jan 2017.*

25. Meena Panchore, Jawar Singh and Saraju P. Mohanty, "Impact of Channel Hot Carrier Effect in Junction- and Doping-Free Devices and Circuits", *IEEE Transactions on Electron Devices, vol.63, no.12, Oct 2016 (IF 2.93).*

24. Kanchan Cecil, and Jawar Singh, "Influence of Germanium source on dopingless tunnel-FET for improved analog/RF performance", *Superlattices and Microstructures (Elsevier), Vol 96, November 2016 (IF 2.13).*

23. Abhishek Sahu, Lokesh Kumar Bramhane and Jawar Singh, "Symmetric Lateral Doping-free BJT: A Novel Design for Mixed Signal Applications", *IEEE Transactions on Electron Devices, vol.67, no.7, May 2016 (IF 2.60).*

22. Lokesh Kumar Bramhane, and Jawar Singh, "Two-zone SiGe base heterojunction bipolar charge plasma transistor for next generation analog and RF applications", *Superlattices and Microstructures (Elsevier), Vol 96, November 2016 (IF 2.13).*

21. Avinash Lahgere, Meena Panchore, and Jawar Singh, "Dopingless Ferroelectric Tunnel FET Architecture for the Improvement of Performance of Dopingless n-Channel Tunnel FETs", *Superlattices and Microstructures (Elsevier), Vol 96, August 2016 (IF 2.13).*

20. Muhammad Khalid and Jawar Singh, "Memristor based unbalanced ternary logic gates", *Analog Integrated Circuits and Signal Processing (Springer), Vol 87 (3), pp 339-406, 2016.*

19. Vishwas Shrivastava, Anup Kumar, Chitrakant Sahu and Jawar Singh, "Temperature sensitivity analysis of dopingless charge-plasma transistor", *Solid-State Electronics (Elsevier), November 2015, ISSN 0038-1101 (IF 1.50).*

18. Deep Kishore Parsediya, Jawar Singh and Pavan Kumar Kankar, "Variable width based stepped MEMS cantilevers for micro or pico level biosensing and effective switching", *Journal of Mechanical Science and Technology (Springer), Vol 29, n0. 11, pp 4823-4832, Nov 2015, 1976-3824 (IF 0.84).*

17. Chitrakant Sahu and Jawar Singh, "Scalability and Process Induced Variation Analysis of Polarity Controlled Silicon Nanowire Transistor", *Journal of Computational Electronics (Springer), August 2015 (IF 1.52).*

16. Avinash Lahgere, Chitrakant Sahu and Jawar Singh, "PVT Aware Design of Dopingless Dynamically Configurable Tunnel-FET", *IEEE Transactions on Electron Devices, vol.62, no.8, August 2015 (IF 2.60).*

15. Chitrakant Sahu and Jawar Singh, "Potential Benefits and Sensitivity Analysis of doping-less Transistor for Low Power Applications", *IEEE Transactions on Electron Devices, vol.62, no.3, pp.729,735, March 2015 (IF 2.60).*

14. Sunil Pandey and Jawar Singh, "A low power and high gain CMOS LNA for UWB applications in 90nm CMOS process", *Microelectronics Journal (Elsevier), Volume 46, Issue 5, May 2015, Pages 390-397 (IF 0.91).*

13. Avinash Lahgere, Chitrakant Sahu and Jawar Singh, "An Electrically Doped Dynamically Configurable Field Effect Transistor for Low Power and High Performance Applications", *Electronics Letters, IET-UK (August 2015) (IF 1.15).*

12. LK Bramhane, N Upadhyay, JR Veluru and Jawar Singh, "Symmetric bipolar charge-plasma transistor with extruded base for enhanced performance", *Electronics Letters, IET-UK (June 2015) (IF 1.15).*

11. Sunil Pandey and Jawar Singh, "A 0.6V low-power and high-gain ultra-wideband low-noise amplifier with forward-body-bias technique for low-voltage operations", *IET-UK Microwaves, Antennas & Propagation, Volume 9, Issue 8, pp 728 - 734 2015, (IF 0.91).*

10. Chitrakant Sahu and Jawar Singh, "Charge-Plasma Based Process Variation Immune Junctionless Transistor", *Electron Device Letters, IEEE, Volume 35, Issue 3, pp 411 - 413, 2014/3 (IF 3.05).*

9. Chitrakant Sahu, Ajanta Ganguly and Jawar Singh, "Design and Performance Projection of Symmetric Bipolar Charge-plasma Transistor on SOI", *IET-UK, Electronics Letters, IET-UK (Sept. 2014) (IF 1.15).*

8. Anup Shrivastava, Komal Singh and Jawar Singh, "Improved Dual Sided Doped Memristor: Modeling and Applications", *IET-UK, Journal of Engineering (April 2014).*

7. Deep Kishore Parsediya, Jawar Singh and Pavan Kumar Kankar, "Simulation and Analysis of Highly Sensitive MEMS Cantilever Designs for "in vivo Label Free" Biosensing", *Elsevier, Vol 14, Journal Procedia Technology, 2014/12/31.*

6. Chitrakant Sahu and Jawar Singh, "Device and Circuit Performance Analysis of Double Gate Junctionless Transistors at Lg=18nm", *IET-UK, Journal of Engineering (Feb 2014).*

5. Chitrakant Sahu, Pragya Swami, S Sharma and Jawar Singh, "Simplified Drain Current Model for Pinch-off Double Gate Junctionless Transistor", *IET-UK, Electronics Letters, IET-UK , Jan 2014, V 50/2 (IF 1.15).*

4. Jawar Singh and N. Vijaykrishnan, "A highly reliable NBTI Resilient 6T SRAM cell", *Microelectronics Reliability (Elsevier), Volume 53, Issue 4, April 2013, Pages 565-572, ISSN 0026-2714 (IF 1.28).*

3. Saraju P. Mohanty, Jawar Singh, Elias Kougianos, and Dhiraj K. Pradhan, "Statistical DOE-ILP Based Power-Performance-Process P3) Optimization of Nano-CMOS SRAM", *Integration, the VLSI Journal (Elsevier), Volume 45, Issue 1, January 2012, Pages 33–45, ISSN 0167-9260 (IF 0.72).*

2. Jawar Singh, Dhiraj K. Pradhan, Simon Hollis and Saraju P. Mohanty, "A single ended 6T SRAM cell design for ultra-low-voltage applications", *Journal of Institute of Electronics, Information and Communication Engineers (IEICE), Japan, Vol. 5 (2008), No. 18 pp. 750-755.*

1. Jawar Singh and R.S Anand, "Computer aided analysis of phonocardiogram", *Journal of Medical Engineering & Technology, 2007, Vol. 31, No. 5 , Pages 319-323.*

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5. Abhash Kumar, Jawar Singh, Sai Manohar Beeraka, and Bharat Gupta, "In-memory Implementation of On-chip Trainable and Scalable ANN for AI/ML Applications", *arXiv preprint arXiv:2005.09526, 2020/19/05.*

4. Md. Hasan Raza Ansari and Jawar Singh, "Improvement in Retention Time of Capacitorless DRAM with Access Transistor", *arXiv preprint arXiv:1910.03907, 2019/10/09.*

3. Alok Kumar Kamal and Jawar Singh, "Ultra-Low Energy and High Speed LIF Neuron using Silicon Bipolar Impact Ionization MOSFET for Spiking Neural Networks", *arXiv preprint arXiv:1909.00669, 2019/09/02.*

2. Kanchan Cecil and Jawar Singh, "Electrostatically Doped Heterojunction TFET with Enhanced Driving Capabilities for Low Power Applications", *arXiv preprint arXiv:1512.06232, 2015/12/19.*

1. Chitrakant Sahu, Avinash Lahgere and Jawar Singh, "A Dynamically Configurable Silicon Nanowire Field Effect Transistor based on Electrically Doped Source/Drain", *arXiv:1412.4975, 12/2014, pp 2.*

CONFERENCE PAPERS

40. Yasin Khan, Pritam Khan, Sudhir Kumar, Jawar Singh and Rajesh Hegde , "Blockchain-based Interoperable Healthcare Using Zero-knowledge Proofs and Proxy Re-Encryption", *17th IEEE India Council International Conference (INDICON), IEEE, New Delhi, India, 2020/12, INDIA.*

39. Bhavye Sharma, Raju Halder, and Jawar Singh, "Blockchain-based Interoperable Healthcare Using Zero-knowledge Proofs and Proxy Re-Encryption", *IEEE International Conference on COMmunication Systems & NETworkS (COMSNETS), 2020, INDIA.*

38. Sandeepkumar Pandey, Jawar Singh, and Pramod K. Tiwari , "Energy and Area Aware Digital Fingerprint Generator Using Intrinsic Randomness", *25th IEEE international conference on noise and fluctuations, June 2019, Neuchâtel (Switzerland).*

37. Deb Deep, Jawar Singh, and Jimson Mathew, "Hardware-Software Co-design Approach for Deep Learning Inference", *7th International Conference on Smart Computing & Communications, June 2019, Malaysia.*

36. Nawaz Shafi, Chitrakant Sahu, C Periasamy, and Jawar Singh, "SiGe Source Charge Plasma TFET for Biosensing Applications", *2017 IEEE International Symposium on Nanoelectronic and Information Systems, pp 93-98, 18/12/2017, Bhopal, INDIA.*

35. Venkata P Yanambaka, Saraju P Mohanty, Elias Kougianos, Prabha Sundaravadivel and Jawar Singh, "Reconfigurable Robust Hybrid Oscillator Arbiter PUF for IoT Security Based on DL-FET", *2017 IEEE Computer Society Annual Symposium on VLSI (ISVLSI), pp 665-670, 3/7/2017, Bochum, Germany.*

34. Venkata P Yanambaka, Saraju P Mohanty, Elias Kougianos, Prabha Sundaravadivel and Jawar Singh, "Dopingless Transistor Based Hybrid Oscillator Arbiter Physical Unclonable

Function", *2017 IEEE Computer Society Annual Symposium on VLSI (ISVLSI), pp 609-614, 3/7/2017, Bochum, Germany.*

33. Venkata P Yanambaka, Saraju P Mohanty, Elias Kougianos and Jawar Singh, "Secure Multi-key Generation Using Ring Oscillator Based Physical Unclonable Function", *2016 IEEE International Symposium on Nanoelectronic and Information Systems, pp 200-205, 19/12/2016, Gwalior, INDIA.*

32. Meena Panchore, Jawar Singh, Saraju P Mohanty, and Elias Kougianos , "Compact Behavioral Modeling and Time Dependent Performance Degradation Analysis of Junction and Doping Free Transistors", *2016 IEEE International Symposium on Nanoelectronic and Information Systems, pp 194-199, 19/12/2016, Gwalior, INDIA.*

31. Chaitanya Maradana and Jawar Singh, "Proposal of Heterogate Technique for Performance Enhancement of DM-TFET", *2016 IEEE International Symposium on Nanoelectronic and Information Systems, pp 118-123,19/12/2016, Gwalior, INDIA.*

30. Muhammad Khalid and Jawar Singh, "Memristor Crossbar-Based Pattern Recognition Circuit Using Perceptron Learning Rule", *2016 IEEE International Symposium on Nanoelectronic and Information Systems, pp 236-239, 19/12/2016, Gwalior, INDIA.*

29. Kanchan Cecil and Jawar Singh, "Performance Enhancement of Dopingless Tunnel-FET Based on Ge-Source with High-k", *2015 IEEE International Symposium on Nanoelectronic and Information Systems, pp 19-22, Indore, INDIA.*

28. Lokesh Kumar Bramhane and Jawar Singh, "Extended Base Schottky-Collector Bipolar Charge Plasma Transistor", *2015 IEEE International Symposium on Nanoelectronic and Information Systems, pp 137-140, Indore, INDIA.*

27. Saurabh Bhaskar and Jawar Singh, "Process variation immune dopingless dynamically reconfigurable FET", *Electron Devices and Solid-State Circuits (EDSSC), 2015 IEEE International Conference on, pp 257-260, Singapore.*

26. Anup Kumar, Chitrakant Sahu and Jawar Singh, "Subthreshold Analog/RF performance estimation of doping-less DGFET for ULP applications", *Emerging Electronics (ICEE), 2014 IEEE 2nd International Conference on, pp 1-4, IISC Bangalore, INDIA, 2014/12/3.*

25. Rajesh Singh Lodhi, Som Dutt Pandey, Chitrakant Sahu and Jawar Singh, "Performance comparison of bulk and SOI planar junctionless SONOS memory", *Emerging Electronics (ICEE), 2014 IEEE 2nd International Conference on, pp 1-4, IISC Bangalore, INDIA, 2014/12/3.*

24. Deep Kishore Parsediya Jawar Singh and Pavan Kumar Kankar, "Modeling and simulation of variable thickness based stepped MEMS cantilever designs for biosensing and pull-in voltage optimization", *2014 VLSI Design and Test, 18th International Symposium on (VDAT), INDIA, 2014/7/16.*

23. Sachin Agrawal, Sunil Kumar Pandey, Jawar Singh and Manoj S Parihar, "Realization of efficient RF energy harvesting circuits employing different matching technique", *2014 IEEE Fifteenth International Symposium on Quality Electronic Design (ISQED), pp 754-761 CA, USA, 2014/3/3.*

22. Anup Shrivastava and Jawar Singh, "Dual-sided doped memristor and it's SPICE modelling for improved electrical properties", *2014 IEEE Fifteenth International Symposium on Quality Electronic Design (ISQED), pp 317-322, CA, USA, 2014/3/3.*

21. Komal Singh, Chitrakant Sahu and Jawar Singh, "Linearly separable pattern classification using memristive crossbar circuits", *2014 IEEE Fifteenth International Symposium on Quality Electronic Design (ISQED), pp 323-329, CA, USA, 2014/3/3.*

20. Anup Shrivastava and Jawar Singh, "Dual sided doped memristor and it's mathematical modelling", *Electronics, Circuits, and Systems (ICECS), 2013 IEEE 20th International Conference on, pp 49-51, Abu Dhabi, 2013/12/8.*

19. Pankaj Kumar, Chitrakant Sahu, Anup Shrivastava, Jawar Singh, and P.N. Kondekar, "Characteristics of gate inside junctionless transistor with channel length and doping concentration", *Electron Devices and Solid-State Circuits (EDSSC), 2013 IEEE International Conference of, pp 1-2, Hong Kong, 2013/6/3.*

18. Chitrakant Sahu, Jawar Singh, and P.N. Kondekar, "Investigation of ultra-thin BOX junctionless transistor at channel length of 20 nm", *Electron Devices and Solid-State Circuits (EDSSC), 2013 IEEE International Conference of, pp 1-2, Hong Kong, 2013/6/3.*

17. Sachin Agrawal, Sunil Pandey, Jawar Singh, and P.N. Kondekar, "An Efficient RF Energy Harvester with Tuned Matching Circuit", *2013 VLSI Design and Test, pp 138-145, INDIA, 2013/1/1.*

16. GK Reddy, Kapil Jainwal, Jawar Singh, and Saraju P Mohanty, "Process variation tolerant 9T SRAM bitcell design", *2012 IEEE Thirteenth International Symposium on Quality Electronic Design (ISQED), pp 493-497, CA, USA, 2012/3/19.*

15. Jawar Singh, Dilip S Aswar, Saraju P Mohanty, Dhiraj K Pradhan, "A 2-port 6T SRAM bitcell design with multi-port capabilities at reduced area overhead", *2010 IEEE Eleventh International Symposium on Quality Electronic Design (ISQED), pp 131-138, CA, USA, 2010/3/22.*

14. A Ricketts, Jawar Singh, K Ramakrishnan, N Vijaykrishnan, D K Pradhan, "Investigating the impact of NBTI on different power saving cache strategies", *2010 ACM-IEEE Design, Automation & Test in Europe Conference & Exhibition (DATE), pp 592-597, Germany, 2010/3/8.*

13. Jawar Singh, Krishnan Ramakrishnan, S Mookerjea, Suman Datta, Narayanan Vijaykrishnan, D Pradhan, "A novel si-tunnel FET based SRAM design for ultra low-power 0.3 VV DD applications", *2010 ACM-IEEE Proceedings of the Asia and South Pacific Design Automation Conference (ASP-DAC), pp 181-186, 2010/1/18.*

12. S Mookerjea, D Mohata, R Krishnan, Jawar Singh, A Vallett, A Ali, T Mayer, V Narayanan, D Schlom, A Liu, S Datta, "Experimental demonstration of 100nm channel length In 0.53 Ga 0.47 As-based vertical inter-band tunnel field effect transistors (TFETs) for ultra low-power logic and SRAM applications", *2009 IEEE International Electron Devices Meeting (IEDM), pp 1-3, 2009/12/7.*

11. Jawar Singh, Dhiraj K Pradhan, Simon Hollis, Saraju P Mohanty, J Mathew, "Single ended 6T SRAM with isolated read-port for low-power embedded systems", *2009 ACM-IEEE Design,*

Automation & Test in Europe Conference & Exhibition (DATE), pp 917-922, Germany, 2009/4/20.

10. Jawar Singh, Jimson Mathew, Saraju P Mohanty, Dhiraj K Pradhan, "Single ended static random access memory for low-vdd, high-speed embedded systems", *2009 22nd International Conference on VLSI Design (VLSID), pp 307-312, INDIA, 2009/1/5.*

9. Yi Xin Su, Jimson Mathew, Jawar Singh and Dhiraj K Pradhan, "Pseudo parallel architecture for AES with error correction", *2008 21st IEEE International SOC Conference (SOCC), pp 187-190, CA, USA, 2008/9/17.*

8. Jawar Singh Jimson Mathew, Dhiraj K Pradhan, Saraju P Mohanty, "Failure analysis for ultra low power nano-CMOS SRAM under process variations", *2008 21st IEEE International SOC Conference (SOCC), pp 187-190, CA, USA, 2008/9/17.*

7. Jawar Singh Jimson Mathew, Dhiraj K Pradhan, Saraju P Mohanty, "A subthreshold single ended I/O SRAM cell design for nanometer CMOS technologies", *2008 21st IEEE International SOC Conference (SOCC), pp 243-246, CA, USA, 2008/9/17.*

6. Jimson Mathew, Jawar Singh, Anas Abu Taleb Dhiraj K Pradhan, "Fault tolerant reversible finite field arithmetic circuits", *2008 14th IEEE International On-Line Testing Symposium (IOLTS), pp 188-189, Rhodes, Greece, 2008/7/7.*

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4. Jimson Mathew,Jawar Singh, Abusaleh M Jabir, Mohammad Hosseinabady, Dhiraj K Pradhan, "Fault tolerant bit parallel finite field multipliers using LDPC codes", *2008 IEEE International Symposium on Circuits and Systems (ISCAS), pp 1684-1687,Seattle, USA, 2008/5/18.*

3. Babita R Jose, P Mythili,Jawar Singh, Jimson Mathew, "A Triple-Mode Sigma-Delta Modulator Design for Wireless Standards", *2007 IEEE 10th International Conference on Information Technology,(ICIT 2007), pp 127-132,INDIA, 2007/12/17.*

2. Jawar Singh, J Mathew, M Hosseinabady, DK Pradhan, "Single event upset detection and correction", *2007 IEEE 10th International Conference on Information Technology,(ICIT 2007), pp 127-132,INDIA, 2007/12/17.*

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JOURNAL EDITORIAL AND REVIEWER ACTIVITIES

- Editor, "IETE Technical Review", *2019.*
- Chair, "IEEE Patna Subsection", *2019-22.*
- Associate Editor, "IEEE TCVLSI VLSI Circuits and Systems Letter", *2016.*
- Associate Editor, "IET Electroics Letters", *2016-19.*

- Reviewer NATURE Scientific Reports
- Reviewer IEEE Transaction on VLSI
- Reviewer IEEE Transaction on Nanotechnology
- Reviewer IEEE Transaction on Electron Devices
- Reviewer IEEE Transaction on Circuits and Systems II (TCAS-II)
- Reviewer IEEE Transactions on Device and Materials Reliability (TDMR)
- Reviewer IEEE Transactions on Emerging Topics in Computing
- Reviewer IEEE/IET Electronics Letters
- Reviewer Elsevier, Transaction on Computers & Electrical Engineering
- Reviewer Elsevier, Superlattices and Microstructures
- Reviewer Elsevier, Microelectronics Journal

CONFERENCE ORGANIZING ACTIVITIES

- General Chair, IEEE International Symposium on Nano-electronic and Information Systems (iNIS 2017), Bhopal, INDIA.
- Student Research Forum Chair, IEEE International Symposium on Nano-electronic and Information Systems (iNIS 2016), Gwalior, INDIA.
- Reviewer Several IEEE and ACM Sponsored/Technical Co-Sponsoted International Conferences, such as DAC, DATE, VLSID, ASP-DAC, ISQED, GLSVLSI, ASQED.
- Track Chair (NVS), IEEE International Symposium on Nano-electronic and Information Systems (iNIS 2015), Indore, INDIA.
- Track Chair, Asia Symposium on Quality Electronic Design (ASQED 2015), Kuala Lumpur, Malaysia.
- Technical Program Committee (TPC) member, The International Symposium on Quality Electronic Design (ISQED) Santa Clara, CA, USA, 2014.
- Technical Program Committee (TPC) member, Interdisciplinary Engineering Design Education Conference, Santa Clara, CA, USA, 2014.
- General Chair, International Conference on "Control, Automation, Robotics and Embedded System" CARE 2013, Dec. 16-18, 2013, IIITDM Jabalpur, INDIA
- Technical Program Committee (TPC) member, The International Symposium on Quality Electronic Design (ISQED) Santa Clara, CA, USA, 2013.
- Technical Program Committee (TPC) member, Interdisciplinary Engineering Design Education Conference, Santa Clara, CA, USA, 2013.

- Session Chair, IEEE Conference on Electrical, Electronics and Computer Sciences, MANIT Bhopal, INDIA, 2012
- Technical Program Committee Member, International Symposium on Electronic System Design (ISED), Kochi, INDIA, 2011
- Technical Program Committee Member, International Symposium on Electronic System Design (ISED), Bhubaneswar, INDIA, 2010

ADMINISTRATIVE ACTIVITIES

- Vice Chairman JEE (Advance), IIT Patna: 2021
- Professor In-Charge: Continuing Education Program, IIT Patna (2019–2021)
- Professor In-Charge: Institute Security, IIT Patna (2018–2019)
- Coordinator: Quality Improvement Program (QIP), IIITDM Jabalpur (2016–2017)
- Coordinator/Head: Mechatronics (PG Program), IIITDM Jabalpur (2015–2017)
- Member: Campus Advisor Committee (CAC) IIITDM Jabalpur (2016-2017)
- Chairman: Central Purchase Committee, IIITDM Jabalpur (2013–2015)
- Member: Central Purchase Committee, IIITDM Jabalpur (2012– 2013)
- In-Charge: Institute Guest House, IIITDM Jabalpur (2012–2014)

THESES SUPERVISED/PROGRESS [Ph.D.]

1. Neha Kamal, "*Investigation of Junction and Doping Free Devices and Their Applications*" – 201- **Progress**
2. Ankit Sirohi, "*Modeling and Simulation of 2D Materials*" – 201- **Progress**
3. Tripty Kumari, "*Modeling and Simulation of Junctioless TFET/NCFETs*" – 201- **Progress**
4. SandeepKumar Pandey, "*Analog Hardware Security Primitive Circuits: Physically Unclonable Functions (PUF)*" – 201- **Progress**
5. Alok Kamal, "*Modeling and Simulation of Silicon Neuron and Its Applications for AI and Deep Learning* " – 201- **Progress**
6. Kanchan Cecil, "*Investigation of Dopingless Tunnel FET for Low-power and High-performance Applications* " – September, 2021 **Assistant Professor, GEC Jabalpur, MP**
7. Meena Panchore, "*Investigation of aging and reliability issues in junction and doping free devices*" – April , 2019 **Assistant Professor, NIT Patna**
8. Lokesh Kumar Bramhane, "*Performance Projection and Analysis of Dopingless Configurable Bipolar Junction Transistors*" – October, 2018 **Assistant Professor, NIT Goa**

9. Muhammad Khalid, "*Investigation of Some Memristor Model Charactristics for Neuromorphic Applications*" – August, 2017 **Post-Doctoral Fellow at JMI**

10. Chitrakant Sahoo, "*Design and Performance Projection of Process Variation Immune Junctionless Field Effect Transistor*" – September, 2015 **Assistant Professor, NIT Jaipur**

THESES SUPERVISED/PROGRESS [Master]

1. Nisha Devangan, "*Study and Analysis of Charge Plasma Based Dopingless Transistor (DLT) for CMOS Scaling*" – 2017

2. Brij Pal, "*Design, Mathematical Modelling and Control of a Hoverbike*" – 2017

3. Neha Kamal, "*Investigation of Soft Errors in Junction- and Doping-free Field Effect Transistors*" – 2017

4. Bidhan Soni, "*Autonomous UAV : An IoT Implementation*" – 2017

5. Suryabhan Singh Rajput, "*Double Gate Doping Less Architecture of Tunnel FET for biosensing Applications*" – 2016

6. Chaitnya Mardana, "*Proposal and Analysis of Heterogate Dielectrically Modulated TFET Biosensor*" – 2016

7. Abhishek Sahu, "*Design and Analysis of Doping-free Symmetric Lateral BJT for Mixed Signal Applications*" – 2016

8. Shashank Kumar, "*Modeling and Numerical Characterization of Novel MEMS Piezoresistive Microcantilever Biosensors*" – 2015 **Dr M Z Ansari, Co-PI**

9. Udit Narayan Bera, "*Optimization of Sensitivity and Resolution for Atomic Force Microscopy Microcantilever with Piezoresistive Read Out*" – 2015 **Dr M Z Ansari, Co-PI**

10. Saurabh Bhaskar, "*Charge Plasma and Polarity Gate Based Reconfigurable Field-Effect Transistor (FET)*" – 2015

11. Avinash Kumar, "*Design and Analysis of Electrically Configurable Dopingless Field-Effect Transistor (FET)*" – 2015

12. Vishwas Shrivastava, "*Temperature Sensitivity Analysis of Junctionless Transistor (JLFET)*" – 2014/15

13. Rajesh Singh Lodhi, "*Performance Analysis of Bulk and SOI Junctionless SONOS Memory*" – 2014

14. Anup Kumar, "*Analog and RF Performance Enhancement of Junctionless Transistor (JLFET)*" – 2014

15. Som Dutt Pandey, "*Junctionless SONOS Non-volatile Memory Cell Characterization*" – 2014

16. Neeta Rahangdale, "*Design and Analysis of Memristor based Logic Circuits and Pattern Classifier*" – 2014

17. Deep Kishore Parsediya, "*Modelling, Analysis and Simulation of MEMS Cantilever Beams*" – 2014 **Dr P K Kankar, Co-PI**

18. Priyanka Singh, "*Simulation and analysis of junctionless transistor for highly sensitive, low power biomedical sensor applications*" – 2014

19. Ajanta Ganguly, "*Simulation, optimization and performance comparison of charge plasma and bipolar transistors*" – 2014

20. Anil Sharma, "*Modelling and Analysis of Diaphragm based MEMS Capacitive Pressure Sensor*" – 2013

21. Anup Shrivastava, "*Modelling, Simulation and Application of Dual-sided Doped Memristor*" – 2013

SUBJECTS TAUGHT

- Semiconductor Devices and Circuits
- Analog & Mixed Signal Systems
- Digital System Design
- CMOS Memory System Design
- VLSI-IC Design
- Microprocessors and Interface
- Sensors and Actuators
- Advanced micro and nano Devices/Nanoelectronics
- Measurement and Instrumentation
- Power Electronics
- Concepts of Electronics Engineering

Jawar Singh,
Patna, INDIA
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