Bio-Data
Santosh Biswas

Name	**SANTOSH BISWAS**
Date of birth	**5th Feb. 1979**
Institute	**IIT Bhilai**
Present position with date of joining	**Professor and Asso. HoD of EECS Dept. in IIT Bhilai**

Summary of educational qualifications:

Sl	Name of the Board / University / Institution and Department	Examination / Degree / Diploma passed	Discipline/ Specialization	Year of Passing	Distinction / Class / Division and CPI / Percentage
1	IIT Kharagpur	PhD	CSE	**Date of Thesis Submission:** 12/4/2008 **Date of Defence** 27/11/2008	--
2	IIT Kharagpur	MS(by Research)	EE	2004	**10.0/10.0 CPI**
3	REC Durgapur (now NIT)	B.E	CSE	2001	79.7%(1st Hons and 3rd position in the Departmen)
4	CBSE	AISSCE	-	1997	1st (80.2%)
5	CBSE	AISSE	-	1995	1st (83.2%)

Particulars of present and past employments:

Sl. No.	Organisation / Institute	Position held	Nature of duties / work	Date of joining	Date of leaving
1	IIT Bhilai	Professor and HoD EECS Dept.	Teaching, Research and Institute level administrative works	30th August 2020	Till date
2	IIT Bhilai	Visiting Asso. Prof. and Associate HoD EECS Dept.	Teaching, Research and Institute level administrative works	14th June 2018	29th August 2020
3	IIT Guwahati	Asso. Prof.	Teaching, Research and departmental level administrative works	22nd March 2014	29th August 2020
4	IIT Guwahati	Asst. Prof.	Teaching, Research and departmental level administrative works	28th November 2008	March 2014
5	IIT Guwahati	Senior Lecturer	Teaching, Research and departmental level administrative works	28th June 2008	27th November 2008
6	SRIC, IIT Kharagpur, Project sponsor: Advanced VLSI Design lab.	Research consultant	Research, CAD tool development Test infrastructure development , VLSI Chip design and test	April 2008	June 2008 (After Submission of PhD Thesis)
7	SRIC, IIT Kharagpur, Project sponsor: Advanced VLSI Design lab.	Research consultant	Research, CAD tool development Test infrastructure development , VLSI Chip design and test	January 2002	April, 2008 (Concurrently while pursuing MS and PhD)
	SRIC, IIT Kharagpur, Project sponsor: National	Research consultant	CAD tool for Analog Placement	May 2005	May 2006 (Concurrently

	Semiconductor Corporation, USA		and Routing		while pursuing PhD)

Teaching Experience:

		Courses taught at IIT Guwahati				
		Sl.	Name of Course	PG/UG	Class strength (approx.)	No. of times taught
		1.	Theoretical Foundation of Computer System	PG	45	2
		2.	CAD for VLSI	PG+UG	90	2
		3.	Systems Programming Lab.	UG	90	8
		4.	Systems Software Lab.	UG	90	8
		5.	VLSI Design, Test and Verification	PG+UG	50	3
		6.	Compilers	UG	90	2
		7.	Compilers Lab.	UG	90	2
		8.	Digital Logic and Computer Architecture	Minor (UG)	30	1
		9.	Computer Organization & Architecture	UG	140	4
		10.	Digital Design	UG	140	4
Courses taught at IIT Bhilai						
		1	Computer Networks	UG	80	1

	Courses taught at other institutes/ on-line/ NPTEL and MOOCS					
		Sl.	Name of Course	PG/UG	Class strength (approx.)	Remarks
		1.	Computer Systems	UG	60	At IIIT Guwahati as a part of mentorship program
		2.	Data Structures	UG	60	
		3.	VLSI Design Verification and Test	PG+UG	--	NPTEL web course
		4.	Design Verification and Test of Digital VLSI Circuits	PG+UG	-	NPTEL video course
		5.	VLSI Design Verification and Test	PG+UG	2500	NPTEL MOOCS

		6.	Computer Organization and Architecture: A Pedagogical Aspect	UG	6500	NPTEL MOOCS
		7	Optimization Techniques for Digital VLSI Design	PG+UG	2500	NPTEL MOOCS
		8	Computer Organization and Architecture	UG	--	Under "Pedagogical Methods" ICT project

Administrative responsibilities (IIT Guwahati)

Institute level	1.	Institute core committee member for peer review and ranking (**including NIRF**) 2016--
	2.	Expert Review member of Technology Incubation Centre, IIT Guwahati. 2015-2017
Departmental level	1.	Departmental Time Table In-charge 2008
	2.	Departmental Under Graduate Program Committee Chair 2009-2012
	3.	Dept. Admission committee core member. 2015-2017
	4.	Departmental Post Graduate Program Committee Chair: 2017--
	5	Dept. representative for ISRO centre 2017--

Administrative responsibilities (IIT Bhilai)

Institute level	1.	Member of the Senate
	2.	Member of Advisory Committee to look after the issues of staffs of IIT Bhilai
	3.	Member/Chair of Faculty and Staff recruitment Committees
	4.	Member of Medical Board Advisory Committee
Departmental level	1.	HoD of EECS Department

PhD and PG Supervision

Ph.D. Supervision					
Sl.	Name of the Student	Area/Title	Period		Present Status
			From	To	
1.	*Neminath Hubballi (IIT Guwahati) Co-Supervisor*	*Design of Network Intrusion Detection Systems: An Effective Alarm Generation Perspective*	*2008*	*2012*	*Associate prof. at IIT Indore*
2.	*Ferdous A. Barbhuiya (IIT Guwahati) Co-Supervisor*	*Design and Development of Intrusion Detection System: A Discrete Event System Approach*	*2009*	*2013*	*Asso. prof. at IIIT Guwahati*
3.	Pradeep Kumar Biswal *(IIT Guwahati) Sole Supervisor*	Decision Diagrams Based On-line Testing of Digital VLSI Circuits	2012	2017	Asst. prof. at IIIT Bhagalpur
4.	Mayank Agarwal *(IIT Guwahati) Main Supervisor*	Intrusion Detection System for Attacks in Wi-Fi Networks: A Discrete Event System Approach	2012	2017	Asst. prof. IIT Patna
5.	Biswajit Bhowmik *(IIT Guwahati) Main Supervisor*	Performance-Aware Test-Time Optimization Schemes of Analysis of Logic Level Faults in Channels of On-Chip Networks	2014	2017	Asst. Prof. NIT Surathkal
6.	Basant Subba *(IIT Guwahati) Co-Supervisor*	On improving the efficacy of intrusion detection systems using game theoretic approaches	2014	2018	Asst. prof. at NIT Hamirpur
7.	Mousum Handique *(IIT Guwahati) Co-Supervisor*	VLSI Testing of reversible circuits	2011	2020	Asst. prof. at Assam University
8.	Amrita Bose Paul *(IIT Guwahati) Main Supervisor*	Intrusion Detection Systems for Wireless Mesh Networks	2009	2019	*Associate Professor, In AEC Guwahati*
9.	*Piyoosh P (IIT Guwahati) Co-Supervisor*	Discrete Event Systems for Scheduling of Embedded Systems	*2014*	*2020*	Asst. prof. at Kerala University

10.	*Rajesh Devaraj (IIT Guwahati) Co-Supervisor*	Discrete Event System Approaches for RT Scheduler Design for Safety-critical Systems	*2014*	*2018*	*Nvidia, Bangalore*
11.	*Pradeep Kumar Sharma (IIT Guwahati) Main-Supervisor*	*Discrete Event Systems and High Level VLSI Testing (*Tentative area)	*2014*	--	
12.	*Vasudevan M.S (IIT Guwahati) Main-Supervisor*	Enhancement of SBST Techniques for Detection of Processor Faults	*2014*	*2020*	*Defence Scheduled on June 2020*
13.	*Surajit Das (IIT Guwahati) Co-Supervisor*	*Discrete Event Systems and High Level VLSI Testing (*Tentative area)	*2014*	--	
14.	*Sisir Kumar Jena (IIT Guwahati) Main-Supervisor*	*Approximate VLSI Testing (*Tentative area)	*2015*	--	
15.	*Nanu Alan Kachari (IIT Guwahati) Main-Supervisor*	E-education using Virtual Labs. (Tentative area)	*2015*	--	
16	*Abhay Deep Seth (IIT Bhilai) Joint Supervisor*	Formal Approaches for Intrusion Detection Systems for IoT framework (Tentative area)	*2018*	--	
17	*Usha Kiran (IIT Bhilai) Joint Supervisor*	Intrusion Detection Systems for IoT (Tentative area)	*2018*	--	
18	*Vishal Sathawane (IIT Bhilai) Joint Supervisor*	Secured and Scalable E-payment Systems (Tentative area)			

M Tech Guidance

Sl.	Name	Title	Period	
			From	To
1.	Rachuri Sreedhar	False Alarm Reduction in SNORT Using Network Vulnerability Information	2007	2009
2.	Vikrant Kumar Singh	Anomaly Detection through Clustering	2008	2010
3.	Kushagra Misra	FDES Application to On-line Testing of Asynchronous Circuits	2008	2010

4.	Sapna Kushwaha	Detection of Kernel Level Root Kits using Loadable Kernel Modules	2008	2010
5.	Roopa S	Active Detection Mechanism for attacks in Autonomous Systems	2008	2010
6.	Dhrubajyoti Pathak	An Intrusion Detection System for Kaminsky DNS Cache Poisoning	2008	2010
7.	Santosh Kumar	Network Anomaly Detection using One-Class small Hypersphere Support Vector Machine	2008	2010
8.	Rittesh Ratti	Active Detection Mechanism for attacks in Autonomous Systems	2008	2010
9.	Vaibhav Gupta	Detection and Mitigation of Induced Low Rate TCP-targeted attack	2009	2011
10.	Pol Shambho Alias G. Haridas	On-Line VLSI Testing	2009	2011
11.	Vivek S Ramteke	Implementing VLAN Attacks and its Detection	2009	2011
12.	Ripunjoy Sonowal	Specification Based Intrusion Detection System for SHORT-AODV	2010	2012
13.	Ashish Bhandari	DES Based IDS for Throughput Degradation Attack on TCP	2010	2012
14.	Mahasweta Mitra	IDS for ARP Spoofing and NDP attacks using LTL based Discrete Event System Framework	2010	2012
15.	Prithu Banerjee	IDS for ICMP Network Attacks using Failure Diagnosis and Detection Theory of DES	2010	2012
16.	Dasari Srinivas	Online Testing of Digital VLSI circuits for Bridging Faults	2010	2012
17.	Manab Mohan Borah	Attack analysis on AODV with SHORT in Ad-Hoc Wireless Networks	2010	2013
18.	Leuva Pratikkumar Khushalbhai	Hybrid System Approach to Online Fault Detection in Power Converter Circuit (Case Study : DC DC Boost Converter)	2011	2013
19.	Argha Sen	A Discrete Event System Approach To Fault-Tolerant Real-Time Multiprocessor Systems	2011	2013
20.	Prabal Kumar Ghosh	Discrete Event System Approach to Evil Twin Attack Detection	2011	2013
21.	Koushik Konar	Online Testing of Digital Circuit Case Study at Comparator	2012	2014
22.	Kamaljeet Chauhan	Real Time Scheduling strategies with incomplete information using Discrete Event System(DES)	2012	2014

23.	Piyoosh P	Discrete Event System (DES) Approach to Fault Tolerance in Real Time System on Homogeneous and Heterogeneous Multiprocessor Platform	2012	2014
24.	Eyerusalem Dagnew Gebru	Online Test for Reversible Circuit	2013	2015
25.	Berhe Gebrezghiabher Wekelle	Online testing of reversible circuits using M-Out-of-N checker	2013	2015
26.	Mukesh Verma	Handling Security Issue in EEOLSR Using Static Bayesian Game Approach	2013	2015
27.	LT. COL. Mandeep Singh Rai	Detection and Mitigation of Identity Spoofing Attacks and Delba Attack in 802.11e Wireless Networks	2014	2016
28.	Jainendra Kumar	Energy Efficient Migration Aware Proportional Fair Scheduling on Multiprocessor	2015	2017
29.	Sandeep Kumar	Detection of Hidden Malicious Logic in Hardware Design Using Functional Analysis	2015	2017
30.	Partha Pritam Mahanta	A Control Path Based Resource Evaluation Strategy for Malware Detection in Embedded Systems	2015	2017
31.	Ajinkya Sanjay Mankar	NOC Testing and Verification	2016	2018
32.	Pavan Ganesh Jeereddy	NOC Testing and Verification	2016	2018

Sponsored and Consultancy Projects

(11 Projects amounting to 10 Crores INR)

Sl. No.	Title	Agency	Amount	Period		Role
				From	To	
1.	Failure Detection and Diagnosis of Fair Discrete Event Systems and its application to VLSI Circuits and Networks.	IIT Guwahati	2.8 Lakhs	2009	2010	PI
2.	Design, Development and Verification of Network Specific IDS using Failure Detection and Diagnosis Theory of Discrete Event Systems	DIETY, New Delhi	111.78 Lakhs	2009	2011	Co-PI
3.	Development of Framework for Logging and Analysis of Network Traffic to secure IT infrastructure	MCIT at Manipur University, CS dept. at Guwahati	15 Lakhs	2009	2014	PI

	(**Consultancy**)	University, IT dept. at Assam University				
4.	Remote Triggered Digital System Laboratory	MHRD	49 Lakhs	2011	2017	PI
5.	On line Testing of Complex VLSI Circuits using Failure Detection and Diagnosis Theory of Discrete Event Systems	DIETY, New Delhi	124 Lakhs	2013	2017	PI
6	A Software Tool for the Planning and Design of Smart Micro Power Grids	IMPacting Research INnovation and Technology (IMPRINT), MHRD, Govt. of India	202Lakhs	2017	2019	Co-Investigator
7	Information Security Research and Development Centre (ISRDC) under Information Security Education and Awareness (ISEA) Project (Phase-II)	Department of Electronics and Information Technology, Govt. of India	344 Lakhs	2015	2020	Co-Chief Investigator
8	Virtual Lab. Integration (Institute Coordinator IIT Guwahati)	NMICTE under MHRD, Govt. of India	247 Lakhs	2014	2020	Institute Coordinator, IIT Guwahati
9	Virtual Labs Phase-III	NMICTE under MHRD, Govt. of India	15 Crores (total for all the consortium members)	2018	2020	National Lab Development Coordinator for Electrical Engineering
10	Formal Methods for Modeling and verification of Intrusion Detection system in wireless Networks	Interdisciplinary Cyber Physical Systems (ICPS) Programme, (DST), Govt. of India, New Delhi	33.02 Lakhs	2019	2021	Principal Investigator
11	Game Theory Based Intrusion Detection System (IDS) for Cyber Physical System	Interdisciplinary Cyber Physical Systems (ICPS) Programme, (DST), Govt. of India, New Delhi	39.82 Lakhs	2019	2021	Co-Investigator
12	Development of course modules for basic UG education in Hardware Design using Hardware Description Language and FPGAs	Ministry of Electronics and Information Technology, Govt. of India		Under Review		Co-Investigator

13	Center for Excellence in Security of Internet of Things	Department to Telecommunication, Govt. of India		Under Review		Co-Investigator
14	Formal Methods for Modeling and Verification of Intrusion Detection System in IoT framework	Ministry of Electronics and Information Technology, Govt. of India		Under Review		Co-Investigator

Journal Publication

h-index 17 i10-index 52

Total International Journals 50

Citations 1772

(a) **Research Papers in International journals**

1.	**S Biswas**, S Mukhopadhyay, A Patra, "A Formal Approach to On-Line Monitoring of Digital VLSI Circuits: Theory, Design and Implementation", Journal of Electronic Testing: Theory and Applications, Springer, Vol. 21, 2005, pp: 503-538, **Impact factor 0.647.**
2.	**S Biswas**, Dipankar Sarkar, Prodip Bhowal and Siddhartha Mukhopadhyay "Diagnosis of Delay-Deadline Failures in Real Time Discrete Event Models", Proc. of ISA Transactions, Elsevier, Vol. 46, Issue 4, pp: 569-582, 2007,**Impact Factor: 3.394**.
3.	**S Biswas**, D Sarkar, S Mukhopadhyay and A Patra, "Diagnosability Analysis of Discrete Time Hybrid Systems", Asian Journal of Control, Wiley, Vol. 10 Issue 6, pp: 651-665, 2008,**Impact Factor: 1.421.**
4	**S Biswas**, S Mukhopadhyay, A Patra, D Sarkar, "Methodology for low-power design on on-line testers for digital VLSI circuits", International Journal of Electronics, Francis and Taylor, Vol. 95 No. 8, pp: 785-797, 2008,**Impact Factor 0.729.**

	5.	**S Biswas**, Siddhartha Mukhopadhyay, Amit Patra, D Sarkar, "An unified methodology for on-line testing of delay and stuck-at faults in digital VLSI circuits", Journal of circuits, systems and computers, World Scientific Press, Vol. 17 Issue 6, pp: 1069-1089, 2008.
	6.	**S Biswas**, D Sarkar, Siddhartha Mukhopadhyay, Amit Patra "Fairness of transitions in diagnosability analysis of discrete event systems", Journal of discrete event dynamic systems: theory and applications, Vol. 20, No. 3, September 2010, pp 349-376, Springer, **Impact Factor 1.660.**
	7.	**S Biswas**, D Sarkar, Siddhartha Mukhopadhyay, "Diagnosability of Delay-Deadline Failures in Fair Real Time Discrete Event Models", International Journal of Systems Science, Vol. 41, No 7, July 2010, pp 763-782, Taylor and Francis, **Impact factor 2.285.**
	8.	Neminath Hubballi, **Santosh Biswas**, Rupa S, Ritesh Ratti,Sukumar Nandi, ``Disrete Event Systems Approach to LAN Attack Detection", ISA Transactions, Vol 50, No1, Jan 2011, pp 119-130, Elsevier, **Impact Factor: 3.394.**
	9.	N. Hubballi, **S. Biswas**, S. Nandi, "Network Specific False Alarm Minimization", Journal of Security and Communication Networks, Vol. 4, No. 11, pp 1339-1349, 2011, Wiley, **Impact Factor: 1.067.**
	10	Ferdous A Barbhuiya, **Santosh Biswas**, and Sukumar Nandi, " An active host-based intrusion detection system forARP-related attacks and its verification", International Journal of Network Security & Its Applications (IJNSA), Vol.3, No.3, May 2011, page 163-180, AIRCC Press **Impact factor 0.62.**
	11	**Santosh Biswas**, "Diagnosability of Discrete Event System for Temporary Failures", Computers and Electrical Engineering, Vol. 38, No. 6, pp 1534-1549, 2012, Elsevier, **Impact Factor: 1.570.**
	12.	N. Hubballi, **S. Biswas**, S. Nandi, "Towards Reducing False Alarms in Network Intrusion Detection Systems with Data Summarization Technique", Journal of Security and Communication Networks, Vol. 6, No. 3, pp 275-285, Wiley 2013, **Impact Factor: 1.067.**
	13.	R Bhattacharya, **S Biswas**, S Mukhopadhyay, "FPGA based Chip Emulation System for Test Development of Analog and Mixed Signal Circuits: A Case Study of DC-DC Buck Converter", Measurement, Vol. 45, No. 8., pp. 1997-2020, Elsevier, 2012,**Impact Factor: 2.359.**
	14.	S. Chakraborty, F. A Barbhuiya, A. Rai, A. Sur, **S. Biswas** and S. Nandi, " Topology Adaptive Computation of Distributed IDS Set for Detecting Attacks on STP", Journal of Information Assurance and Security, Vol. 7, No. 5., pp. 284-295, 2012.
	15.	A B Paul, S Konwar, S Nandi and **S Biswas**, "Trusted M-OLSR for Secure Routing in Wireless Mesh Networks", Journal of Information Assurance and Security, Vol. 8, No. 1, pp. 17-32, 2013.
	16.	F.A. Barbhuiya, G Bansal, N Kumar, **S. Biswas** and S. Nandi, "Detection of Neighbor Discovery Protocol Based Attacks in IPv6 Network (SPECIAL ISSUE for SIN 2011)", Issue 3-4, Springer, Page 91-113, May 2013
	17.	M. Mitra, P. Banerjee, F. A. Barbhuiya, **S. Biswas** and S. Nandi, "IDS for ARP Spoofing using LTL based Discrete Event System Framework (Special issue for SIN 2011)", Issue 3-4, Networking Science", Springer, 114-134, May 2013.
	18.	M. Agarwal, D. Pasumarthi, **S. Biswas** and S. Nandi, "Machine Learning Approach for Detection of Flooding DoS attacks in 802.11 Networks and Attacker Localization", International Journal of Machine Learning and Cybernetics, Volume 7, Issue 6, pp 1035-1051,**Impact factor 1.699.**

	19.	P. Biswal and **S. Biswas**, "A Polynomial Algorithm for Diagnosability of Fair Discrete Event Systems", Systems Science and Control Engineering, Taylor and Francis, Volume 3, Issue 1, Pages 307-319, 2015 .
	20.	P. Biswal and **S. Biswas**, "A Binary Decision Diagram based Online Testing of Digital VLSI Circuits for Feedback Bridging Faults", Microelectronics Journal, Elsevier, Volume 46, Issue 7, Pages 598-616, 2015, **Impact Factor: 1.163.**
	21.	M. Agarwal, D. Pasumarthi, **S. Biswas** and S. Nandi, Advanced Stealth Man in the Middle Attack in WPA2 Encrypted Wi-Fi Networks", in the IEEE Communications Letters, Vol. 19, No. 4, pp. 581-584, 2015, Impact **Factor 1.988.**
	22.	P K Biswal, K Mishra, **Santosh Biswas** and Hemangee Kapoor, A Discrete Event System Approach to Online Testing of Asynchronous Circuits, Journal of VLSI Design, Hindawi. Article ID 651785, 16 pages, 2015**,Impact factor 0.54.**
	23.	Rajesh D, Arnab Sarkar and **Santosh Biswas**, A Design Fix to Supervisory Control for Fault-tolerant Scheduling of Real-time Multiprocessor Systems with Aperiodic Tasks. International Journal of Control, Taylor & Francis (Vol. 88, No. 11, page 2211-2216), 2015 **Impact Factor: 2.208.**
	24.	F A Barbhuiya, M. Agarwal, S. Purwar, **S. Biswas** and S. Nandi, "Application of Stochastic Discrete Event System Framework for Detection of Induced Low Rate TCP Attack", ISA Transactions, Elsevier, Vol. 58, pp. 474-492, September 2015, **Impact Factor: 3.394.**
	25.	B. Subba, **S. Biswas**, S Karmakar, Intrusion Detection in Mobile Ad hoc Network: Bayesian Game Formulation", Engineering Science and Technology: an International Journal., Elsevier, Volume 19, Issue 2, June 2016, Pages 782-799 .
	26.	PK Biswal, HP Sambho, **S Biswas**, "A Discrete Event System approach to On-line Testing of digital circuits with measurement limitation", Engineering Science and Technology, an International Journal, Volume 19, Issue 3, 2016, Pages 1473-1478 .
	27.	M. Agarwal, S Purwar, **S. Biswas** and S. Nandi, "Intrusion Detection System for PS-Poll DoS Attack in 802.11 Networks using Real Time DES", in the IEEE/CAA Journal of Automatica Sinica, IEEE, Volume: 4, Issue: 4, Pages 792-808,2017 **Impact Factor: 2.16**.
	28.	M. Agarwal, **S. Biswas** and S. Nandi, "Discrete Event System Framework for Fault Diagnosis with Measurement Inconsistency: Case Study of Rogue DHCP Attack, in the IEEE/CAA Journal of Automatica Sinica, IEEE, Volume: PP, Issue: 99, Pages 1-18, 2017 **Impact Factor: 2.16.**
	29.	R. Devaraj, A. Sarkar, **S. Biswas**, " Comments on Supervisory control for real-time scheduling of periodic and sporadic tasks with resource constraints" IFAC Automatica, Volume 82, Pages 332-334 ,2017, **Impact Factor: 5.451**
	30.	R. Devaraj, A. Sarkar, S. Biswas, "Fault-Tolerant Preemptive Aperiodic RT Scheduling by Supervisory Control of TDES on Multiprocessors, ACM Transactions on Embedded Computing Systems (TECS), Volume 16 Issue 3,Pages 87:1-87:25 ,2017,**Impact Factor: 1.367**.
	31.	B. Subba, **S. Biswas**, S Karmakar, "False Alarm Reduction in Signature based IDS: Game Theory Approach, Journal of Security and Communication Networks, Wiley, Volume 9, Issue 18, 2016, **Impact Factor: 1.067.**

	32.	Rahul Bhattacharya, Subindu Kumar, **Santosh Biswas**, " Resource optimization for emulation of behavioral models of mixed signal circuits on FPGA: a case study of DC-DC buck converter ", International Journal of Circuit Theory and Applications, Wiley, Volume 45, Issue 11 , Pages 1701-1741 ,2017 , **Impact Factor: 1.571.**
	33.	Biswajit Bhowmik, Jatindra Kumar Deka, **Santosh Biswas**, "A Time-Optimized Scheme Towards Analysis of Channel-Shorts in on-Chip Networks", "Journal of Electronic Testing: Theory and Applications", Volume 33, Issue 2, pp 227-254, April 2017, Springer , **Impact Factor 0.647.**
	34.	Pradeep Kumar Biswal, **Santosh Biswas**, "On-Line Testing of digital VLSI circuits at Register Transfer Level using High Level Decision Diagrams", "Microelectronics Journal", Volume 67, pp 88-100, August 2017, Elsevier, **Impact Factor: 1.163**.
	35.	Rahul Bhattacharya, Subindu Kumar, **Santosh Biswas**, "Fault Diagnosis in Switched-Linear Systems by Emulation of Behavioral Models on FPGA: A case study of current-mode buck converter", International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, Wiley, 2017, **Impact Factor: 0.622**
	36.	Basant Subba, **Santosh Biswas**, Sushanta Karmakar, "A game theory based multi layered intrusion detection framework for VANET", Future Generation Computer Systems (FGCS), Elsevier Volume 82, 2018, Pages 12-28 , **Impact Factor: 3.997.**
	37.	Amrita Bose Paul, **Santosh Biswas**, Sukumar Nandi, Sandip Chakraborty, "MATEM: An Unified Framework based on Trust and MCDM for Assuring Security, Reliability and QoS in DTN Routing", Journal of Network and Computer Applications (JNCA), Elsevier , Volume 104, 2018, Pages 1-20,**Impact Factor: 3.500 .**
	38.	Biswajit Bhowmik, **Santosh Biswas**, Jatindra Kumar Deka, Bhargab Bhattacharya, "Reliability-Aware Test Methodology for Detecting Short-Channel Faults in On-Chip Networks ", "IEEE Trans. on VLSI systems", IEEE (accepted),**Impact factor 1.698.**
	39.	Vasudevan Madampu Suryasarman, **Santosh Biswas**, A. Sahu "Automation of Test Program Synthesis for Processor Post-silicon Validation", "Journal of Electronic Testing: Theory and Applications", Springer (Accepted) ,**Impact factor 0.647.**
	40	R. Devaraj, A. Sarkar, S. **Biswas**, "Supervisory Control Approach and its Symbolic Computation for Power-aware RT Scheduling", IEEE Trans. on Industrial Informatics, IEEE (accepted), **Impact factor 6.76.**
	41	M. Agarwal, **S. Biswas** and S. Nandi, "An Efficient Scheme to Detect Evil Twin Rogue Access Point Attack in 802.11 Wi-Fi Networks", International Journal of Wireless Information Networks (IJWI) (accepted), **Springer, Impact factor 1.38** .
	42	Basant Subba, **Santosh Biswas**, Sushanta Karmakar " A game theory based multi layered intrusion detection framework for wireless sensor networks ", International Journal of Wireless Information Networks (IJWI) (accepted), Springer, **Impact factor 1.38 .**
	43	P.P. Nair A. Sarkar, **S. Biswas**, "Design of Light Weight Exact DES Diagnosers using Measurement Limitation: Case Study of EFI system", International Journal of Systems Science, Taylor and Francis (accepted), **Impact factor 2.285**.
	44	PK Sharma, **S Biswas**, P Mitra, “Energy Efficient Heuristic Application Mapping for 2-D Mesh-based Network-on-Chip”, Microprocessors and Microsystems, Elsevier, (accepted); **Impact factor 1.049**.

	45	Biswajit Bhowmik, Jatindra Kumar Deka, **Santosh Biswas**, "On-Line Analysis of Stuck-at Faults in On-Chip Network Interconnects", Journal of Circuits, Systems and Computers, Vol. 27, No. 13, 1850203 (2018), World Scientific, **Impact factor 0.595**.
	46	Biswajit Bhowmik; Jatindra Kumar Deka; **Santosh Biswas**; Bhargab B. Bhattacharya," Performance-Aware Test Scheduling for Diagnosing Coexistent Channel Faults in Topology-Agnostic Networks-on-Chip", ACM Transactions on Design Automation of Electronic Systems (TODAES), (Accepted); **Impact factor 0.87**.
	47	Biswajit Bhowmik; **Santosh Biswas**; Jatindra Kumar Deka; Bhargab B. Bhattacharya," A Low-Cost Test Solution for Reliable Communication in Networks-on-Chip" Journal of Electronic Testing: Theory and Applications, Springer (Accepted); **Impact factor 0.87**.
	48	PP Nair, A Sarkar, S Biswas, "Fault-tolerant Real-time Fair Scheduling on Multiprocessor Systems with Cold-standby", IEEE Transactions on Dependable and Secure Computing (Accepted)
	49	VM Suryasarman, S Biswas, A Sahu, "RSBST: an Accelerated Automated Software-Based Self-Test Synthesis for Processor Testing", Journal of Electronic Testing, Springer, 1-20; **Impact factor 0.87**.
	50	P K Biswal and S Biswas "A Binary Decision Diagram Approach to On-line Testing of Asynchronous Circuits with Dynamic and StaticC-elements", Journal of Electronic Testing, Springer,(accepted); **Impact factor 0.87**.
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116	Abhay Deep Seth, Amit Kumar Dhar and Santosh Biswas, “De-Authentication Attack Detection using Discrete Event Systems in 802.11 Wi-Fi Networks”, ”, IEEE ANTS 2019 (Accepted)

Short-term courses / workshops / conferences organized	
Courses / Workshops / Conferences	Year
Seventh Annual Inter Research Institute Student Seminar in Computer Science IIT Guwahati **Program Committee Member**	13th - 14th June 2009
AICTE Sponsored QIP Short Term Course "VLSI Design Verification and Test", IIT Guwahati: **Organizer**	8th - 12th June 2009
AICTE Sponsored QIP Workshop "What is Common among Cloud Computing, Nanotechnology and Green Computing", IIT Guwahati: **Organizer**	19th – 21th January, 2012
Eighth International Conference on Information Systems Security (ICISS 2012), IIT Guwahati, India: **Organizing co-chair**	15-19 December 2012,
Workshop on Xilinx FPGA Architecture and Design flow, at IIT Guwahati: **Co-convener**.	November 22nd-23rd, 2013
Foundations of Software Technology and Theoretical Computer Science (FSTTCS 2013), IIT Guwahati, India: **Chair**	December 10 to 14, 2013,
KIC-TEQIP STC on "Real-Time Embedded Systems - Design, Verification and Test". IIT Guwahati **organizer**	25th Nov. to 1st Dec, 2014
QIP STC on "Computational Methods for Smart Grids", IIT Guwahati **organizer**	9th to 13th March, 2015
KIC-TEQIP Workshop on "Information and Communication Technology in Healthcare: Challenges and Promises", IIT Guwahati **organizer**	25th March, 2015

GAIN course on "MIXED-CRITICALITY REAL-TIME SYSTEMS", IIT Guwahati **organizer**	May 2018,

Awards / Honours etc.	
1.	Nominated as Research Associate in International Academic Exchange of Nan Yang Academy of Sciences (NAS) in Singapore. NAS is a scientific institution registered with the Singapore's Ministry of Education (MOE)
2.	Nominated for Best Paper award in VLSI Design Conference 2019
3.	Recipient of “outstanding Contribution in Reviewing” by Elsevier
4	Recipient of Best Paper Award in IEEE TENCON 2017
5	Recipient of Best Paper Award in IEEE TENCON 2015
6	IEI Young Engineer Award in Computer Science and Engineering 2013-14, The Institutions of Engineers (India)
7	Microsoft Outstanding Young Faculty Program 2008-09.
8	Special Mention by IEEE India Council and IEEE Gujarat Section for contributions in reviewing research papers for INDICON (INDICON is organized by IEEE India Council in the field of Computer Science and Engineering, Electrical Engineering & electronics and Communication Engineering)
9	Masters thesis awarded by Infineon Technologies, INDIA as the best “Masters Thesis in INDIA” published during the year 2004-05.
10.	10/10 CGPA in the Degree M.S awarded by Indian Institute of Technology, Kharagpur. Institute highest CGPA in the year 2004
11	Awarded Merit Scholarship by NIT Durgapur for excellence in Academics for the degree of B.E (Top 10% of the students).